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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/640,961	08/16/2000	Qing Ma	042390.P9556	3719

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EXAMINER

CLARK, SHEILA V

ART UNIT	PAPER NUMBER
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2815

DATE MAILED: 03/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.
09/640,961

Applicant(s)
Ma et al

Examiner
Sheila V. Clark

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE three MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (e). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on Feb 21, 2003
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4 and 24-40 is/are pending in the application.
- 4a) Of the above, claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4 and 24-40 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- *See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____ 6) ☐ Other:

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The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-3 and 25-29, 31-34, 37 rejected under 35 U.S.C. 102(a) as being anticipated by Chung.

Chung et al teaches substantially all of the structural features recited in the claims wherein for example figure 6 Chung shows a microelectronic die 140 having an active top surface and at least one side and encapsulation 150 is shown adjacent one side and said encapsulation includes one lower shoulder surface substantially planar to the die active surface. A first dielectric 146 is shown resting on said shoulder of said encapsulation and is shown formed on said active surface and at least one conductive trace 134, 132, 110 (col. 10 , line 40-50 teaches use of same nickel material) is shown disposed on said first dielectric and in electrical contact with said active surface said die active surface and adjacent said encapsulation. An additional dielectric 120 is shown disposed over said one trace and said at least one trace extends through (132) and resides on (132 and 110) said at least one additional dielectric material layer. A bottom surface of said encapsulation is shown to be planar to the back surface of die 140.

Chung further teaches similar features in Figure 14 whereby Chung shows microelectronic dies 140, 180 and 190 having active top surfaces and at least one side and encapsulation 150 is shown adjacent one side and said encapsulation includes one top surface substantially planar to

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the die active surfaces. A first dielectric 120 is shown resting on said encapsulation and is shown formed on said active surface and at least one conductive trace 133, 132, 114 are shown disposed on said first dielectric and in electrical contact with said active surface and adjacent said encapsulation. An additional dielectric 610 is shown disposed over said one trace and said at least one trace is taught to extend through and resides on said at least one additional dielectric material layer. A bottom surface of said encapsulation is shown to be planar to the back surface of die 140.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 26, 27, 31, 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Fordemwalt et al.

Fordemwalt et al shows a microelectronic device 13 (or a plurality 13-16) having an active surface and an encapsulation 12 adjacent and planar to the die active surface. A first dielectric material 21 is formed on said active surface and at least one conductive trace 25 (22, 23, 24, 26) is taught to be disposed on said dielectric and in electrical contact with said active surface (see col. 4, lines 56-59).

Claims 1, 26, 27 are rejected under 35 U.S.C. 102(a) as being anticipated by Nishihara et al.

Nishihara et al shows a microelectronic device 1 having an active surface and an encapsulation 18 adjacent and planar to the die active surface. A first dielectric material 2 is

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formed on said active surface and at least one conductive trace 4 is taught to be disposed on said dielectric and in electrical contact with said active surface.

Claims 1, 4, 24, 26, 27, 30, 31, 32, 35, 36, 38, 38-40 are rejected under 35 U.S.C. 102(b) as being anticipated by Donovan.

Donovan shows a microelectronic die 12a (a plurality 12b, 12c) having an active top surface and at least one side and encapsulation 28 is shown adjacent one side and said encapsulation includes one surface substantially planar to the die active surface. A first dielectric 123 is shown disposed on said encapsulation and formed on said active surface and at least one conductive trace 32 is shown disposed on said first dielectric and in electrical contact with said active surface said die active surface and adjacent said encapsulation. At least one heat dissipation device 40 is shown in thermal contact with said microelectronic device back surface.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 4, 24, 35, 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung or Nishihara or Fordemwalt et al (as applied above) in view of Donovan et al.

The features of the claims from which claims 4, 24, 35, and 36 depend have been discussed in detail supra except for use of a heat dissipation device in thermal contact with the bottom surface of the microelectronic chip. Donovan teaches a similar device to those of Chung

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or Nishihara or Fordemwalt et al and teaches the use of heat dissipation device 40 formed in thermal contact with the back of microelectronic device 12c (12 a and 12b). Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a heat dissipation device on the bottom surface of the electronic device. The ordinary artisan would have been motivated to modify Chung or Nishihara or Fordemwalt for the purposes of improving or increasing heat dissipation. Further providing the bottom surfaces of electronic devices with heat dissipation structures to improve heat dissipation is well known and performed conventionally in this art.

Claims 1-4, 24-40 are rejected.

Applicant's arguments filed 2-21-2003 taken with arguments of previous actions have been fully considered but they are not persuasive. The references continue to clearly teach the features of the invention as they are recited substantially item for item. Contrary to applicant's assertions in the most recent response, Donovan clearly teaches a and show a heat dissipation device 40 which is shown formed on the back surface of the microelectronic device shown in figure 4. The websites from which the "trace" definition was obtained is <http://www.maxmon.com/et.htm>. Arguments from previous actions are repeated and stand as stated.

Applicant argues that the metal layer 110 of Chung fails to be a trace and fails to be in electrical contact with the active surface of the chip. The definition that the applicant provided (a uniform metal or doped semiconductive structure, a significant portion of which is elongated and runs laterally when viewed in proper cross section) relative to the definition of trace is not deemed

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to be persuasive. Contrary to applicant's argument the well know definition of trace is in this technology is deemed to be only an conductive metal layer which may be electrically conductive.

The various electronic glossaries define trace as, trace-a conducting connection between electronic components.

May also be called a track or a signal. In the case of integrated circuits, such interconnections are often referred to collectively as metalization.

trace- a line or "wire" of conductive material such as copper, silver or gold, on the surface of or sandwiched inside a PCB, printed circuit board. These traces are often called individually a run. Traces carry an electronic signal or other forms of electron flow from one point to another. Traces that are on the surface of a board are covered with a non-conductive coating, except at contact or solder points, to keep unintentional contact from being made with other conductive surfaces.

And further contrary to applicants argument said trace does not have to run in any particular direction (i.e. laterally) and is a conductor not necessarily a semiconductive structure though a trace may be contained in a semiconductor structure and may have semiconductive characteristics. Therefore the office action is deemed to appropriately define components 134, 132 and 110 as traces.

Applicant further argues that "in electrical contact" is well known to mean one structure physically touching another structure". Contrary to applicant's argument two electrical components may be located on different areas of circuit boards or chips and be located in different rooms, buildings, etc. be in electrical contact. Physical contact is not a requirement of being "in electrical contact". "In electrical contact" is a interactive relationship between electrical energy or current, not necessarily physical contact. Trace 110 is clearly in electrical contact with the active surface of chip 140 via trace 132 and trace 132 is show to be in electrical contact with

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chip 140 via metal layer 134 and etc. Also contrary to applicants assertions, col. 5 lines 12-15 of Chung teach that the network of components (integrated circuit and/ or passive components) of chip 140 are attached to metal layer 110.

The features of the instant invention are deemed to be substantially the same and continue to be taught

Contrary to applicant's other arguments such as "dielectric 120 disposed over said one trace". Dielectric 120 is clearly shown to be "disposed over" the rear surface of trace 110, the side surfaces of trace 132 and the top surface of trace 134. Contrary to applicant's view the term "over" does not necessarily mean "on the top surface of". Whereby one definition reads:
over- across a barrier or intervening space.

Further though the office action may have inadvertently described first dielectric 23 as 123 of Donovan and encapsulation 8 as 18 of Nishihara, the office action would by no means be regarded as making said office action incomprehensible to one having ordinary skill in this art. Clearly one of ordinary skill in the art can follow the description of components in the office action and clearly determine and see that a first dielectric 23 is clearly shown connected to trace 32 as described in the office action and chip 1 of Nishihara is clearly shown to be encapsulated by sealing resin 8.

It is believed that the references relied upon in the office action meet the features recited in the instant claims as they are broadly recited substantially item for item. Further the terms argued by the applicant may have a far broader definition than those argued. Features such as a conductor

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running laterally, components physically touching and components located on the top surface argued by the applicant fail to be specifically recited in the claims.

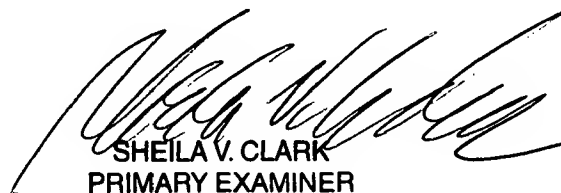
Applicant attempts to take claims that recite broad well known structural features and argue that these well known features are inventive. The claims however continue to recite features that are well known to one having ordinary skill in microelectronic chip technology

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner S.V. Clark whose telephone number is (703) 308-4924.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee, can be reached on (703) 308-1690. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956

March 6, 2003



SHEILA V. CLARK
PRIMARY EXAMINER